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Westby

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(54) **METHOD AND APPARATUS FOR USING CRC FOR DATA INTEGRITY IN ON-CHIP MEMORY**

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(56) **References Cited**

**U.S. PATENT DOCUMENTS**

4,819,229	4/1989	Pratty et al.	370/89
5,168,568	12/1992	Thayer et al.	395/725
5,598,541	1/1997	Malladi	395/286
5,619,497	4/1997	Gallagher et al.	370/394
5,619,647	4/1997	Jardine	395/200.1
5,638,518	6/1997	Malladi	395/200.21
5,819,111	10/1998	Davies et al.	395/849
5,901,280 *	5/1999	Mizuno et al.	395/182.04
6,012,128	1/2000	Birns et al.	711/163

**OTHER PUBLICATIONS**

“Fibre Channel, Arbitrated Loop (FC-AL), Rev 4.5”, American National Standard for Information Technology draft proposed, ANSI X3.272-199 X, (Jun. 1, 1995).

“Fibre Channel, Arbitrated Loop (FC-AL-2), Rev 6.3”, American National Standard for Information Technology draft proposed, ANSI X3.XXX-199x, (May 29, 1998).

“Fibre Channel, Physical and Signaling Interface (FC-PH), Rev 4.3”, American National Standard for Information Systems working draft, ANSI X3.230-199x, (Jun. 1, 1994).

“Information Systems—dpANS Fibre Channel Protocol for SCSI”, American National Standard—draft proposed, X3.269-199x revision 12, (Dec. 4, 1995).

Georgiou, C.J., et al., “Scalable Protocol Engine for High-Bandwidth Communications”, IEEE, pp. 1121-1126, (1997).

\* cited by examiner

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**ABSTRACT**

Cyclic-redundancy-code (“CRC”) information that is received along with a frame from a fiber-channel is stored in an on-chip frame buffer, and later checked to ensure the integrity of the data while in the frame buffer. In various embodiments, data frames, along with their CRC information, are stored into a data-frame buffer, and/or non-data frames along with their CRC information are stored into a receive-non-data-frame buffer. The improved communications channel system includes a channel node having dual ports, each port supporting a fiber-channel arbitrated-loop serial communications channel. The serial communications channels each include CRC on data transmissions on the channel, an on-chip frame memory located on-chip in the channel node that receives a data frame and the frame’s associated CRC from the communications channel, and an integrity apparatus that later uses the received associated CRC for data-integrity checking of data in the on-chip frame memory. In addition, a method for using CRC for data integrity in on-chip memory is described.

17 Claims, 15 Drawing Sheets

